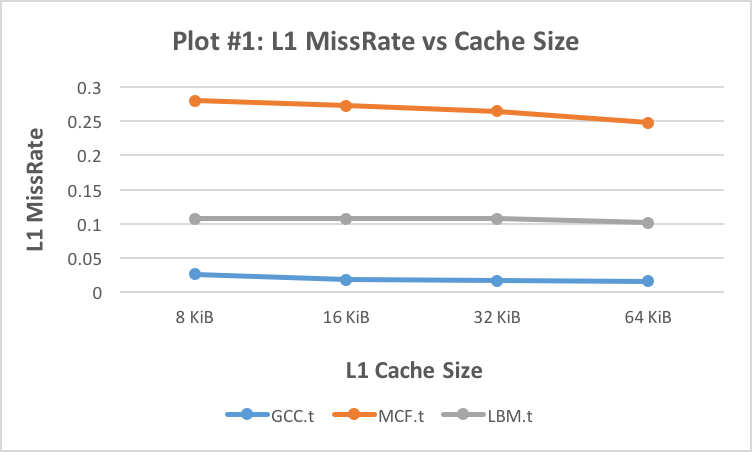
**Exploring the L1 Cache Design:**

**Plot #1:**

Assume that there is no L2 cache. Assume that LRU replacement policy is used for the L1 cache. Fix the L1 block size at 64B and the L1 associativity at 4. Vary the cache size between 8KiB, 16KiB, 32KiB and 64KiB. Plot the L1 cache miss rates. The plot should have 4 data points per benchmark.

|  |  |  |  |
| --- | --- | --- | --- |
|  | **L1 Cache Miss Rates** | | |
| **L1 Cache Size** | **GCC.t** | **MCF.t** | **LBM.t** |
| **8 KiB** | 0.026388 | 0.279413 | 0.107725 |
| **16 KiB** | 0.018553 | 0.272435 | 0.107721 |
| **32 KiB** | 0.0169005 | 0.264445 | 0.107721 |
| **64 KiB** | 0.016156 | 0.247528 | 0.101456 |

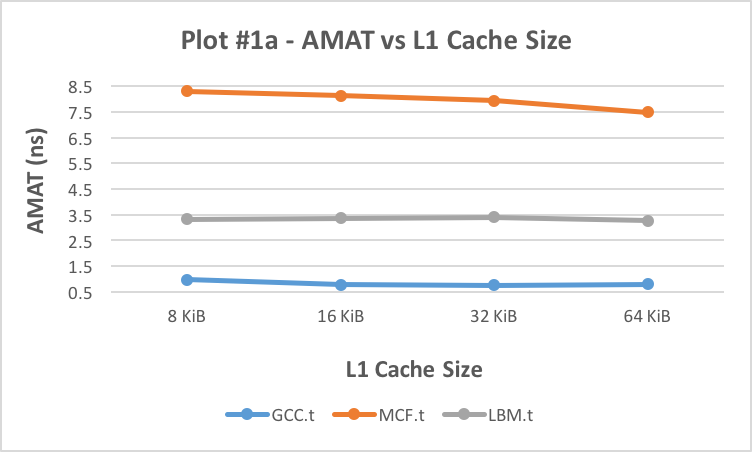


**Miss Penalty = Memory Latency + (Block Size/Memory Bandwidth)**

**= 25ns + 64B/16GB/s = 25ns + 4ns = 29ns**

**AMAT = Hit Time + Miss Rate × Miss Penalty**

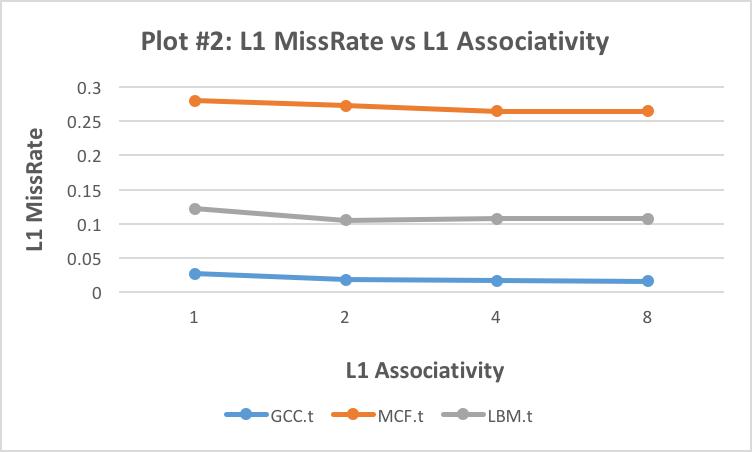
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | **L1 AMAT (ns)** | | |
| **L1 Cache Size** | **Hit Time (ns)** | **GCC.t** | **MCF.t** | **LBM.t** |
| 8 KiB | 0.211173 | 0.976425 | 8.31415 | 3.335198 |
| 16 KiB | 0.233936 | 0.771973 | 8.134551 | 3.357845 |
| 32 KiB | 0.27125 | 0.7613645 | 7.940155 | 3.395159 |
| 64 KiB | 0.319481 | 0.788005 | 7.497793 | 3.261705 |

****

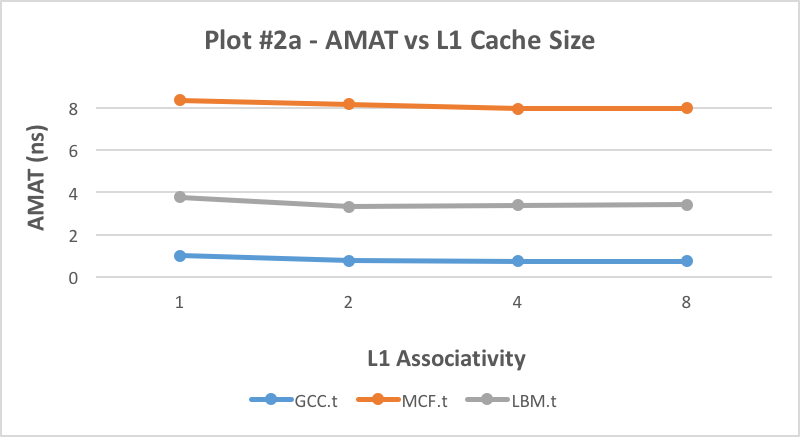
**Plot #2:**

Assume that there is no L2 cache. Assume that LRU replacement policy is used for the L1 cache. Fix the L1 block size at 64B and the L1 cache size at 32KiB. Vary the associativity between 1, 2, 4 and 8. Plot the L1 cache miss rates. The plot should have 4 data points per benchmark.

|  |  |  |  |
| --- | --- | --- | --- |
|  | **L1 Cache Miss Rates** | | |
| **L1 Associativity** | **GCC.t** | **MCF.t** | **LBM.t** |
| **1** | 0.0269015 | 0.279413 | 0.121798 |
| **2** | 0.01819 | 0.272435 | 0.105314 |
| **4** | 0.0169005 | 0.264445 | 0.107721 |
| **8** | 0.0164355 | 0.264424 | 0.107721 |



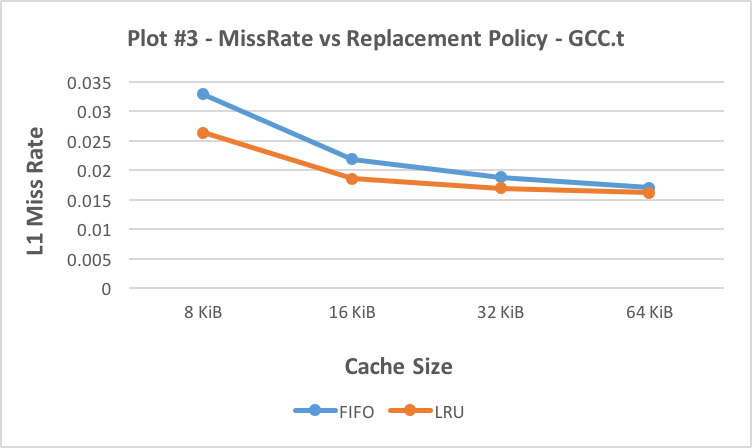
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | **L1 AMAT (ns)** | | |
| **L1 Associativity** | **Hit Time (ns)** | **GCC.t** | **MCF.t** | **LBM.t** |
| 1 | 0.233353 | 1.0134965 | 8.33633 | 3.765495 |
| 2 | 0.262446 | 0.789956 | 8.163061 | 3.316552 |
| 4 | 0.27125 | 0.7613645 | 7.940155 | 3.395159 |
| 8 | 0.288511 | 0.7651405 | 7.956807 | 3.41242 |

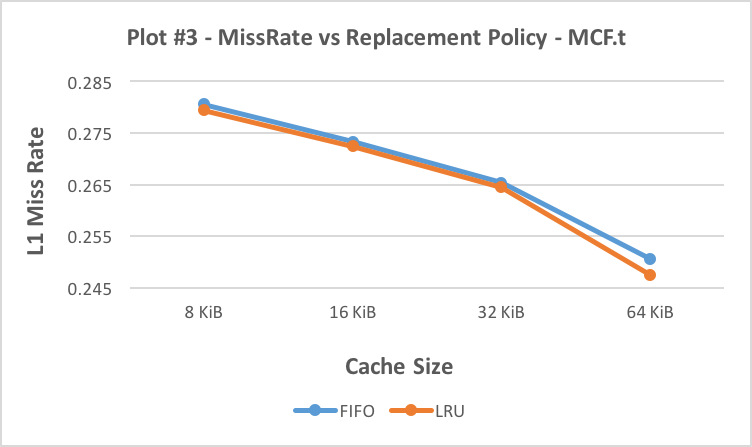


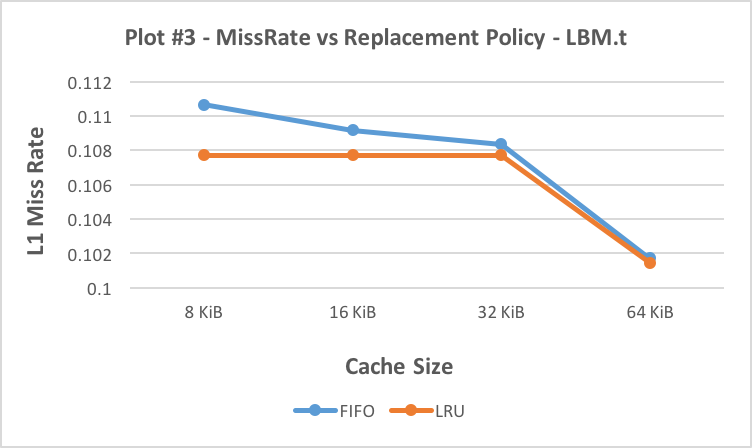
**Exploring the Replacement Policy:**

**Plot #3:**

Assume that there is no L2 cache. Fix the L1 block size at 64B and the L1 associativity at 4. Vary cache size between 8KiB, 16KiB, 32KiB and 64KiB. For each configuration vary the replacement policy between LRU and FIFO. Plot the L1 Cache miss rates for each replacement policy. Note that for each benchmark this plot will have 2 data series (one per replacement policy) and each data series will have 4 data points (one per cache size). That is, 8 data points per benchmark.







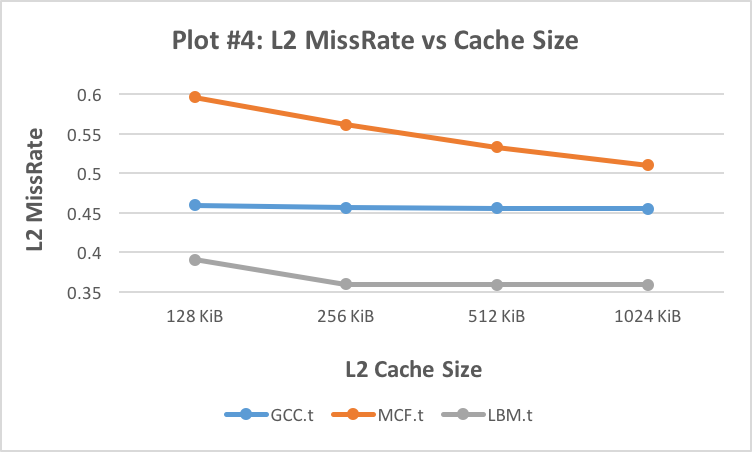
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | **GCC.t** | | **MCF.t** | | **LBM.t** | |
| **L1 Cache Size** | **FIFO** | **LRU** | **FIFO** | **LRU** | **FIFO** | **LRU** |
| **8 KiB** | 0.0328635 | 0.026388 | 0.280598 | 0.279413 | 0.110667 | 0.107725 |
| **16 KiB** | 0.021876 | 0.018553 | 0.273329 | 0.272435 | 0.109162 | 0.107721 |
| **32 KiB** | 0.0187845 | 0.0169005 | 0.265338 | 0.264445 | 0.108364 | 0.107721 |
| **64 KiB** | 0.017017 | 0.016156 | 0.250573 | 0.247528 | 0.101733 | 0.101465 |

**Exploring the L2 Cache Design:**

**Plot #4:**

Fix block size at 64B, L1 cache size at 16KiB, L1 associativity at 4 and the replacement policy to be LRU. Assume that the L2 Cache is always non-inclusive. Fix L2 associativity at 8. Vary the L2 cache size between 128KiB, 256KiB, 512KiB and 1MB. Plot the L2 cache miss rates. The plot should have 4 data points per benchmark.

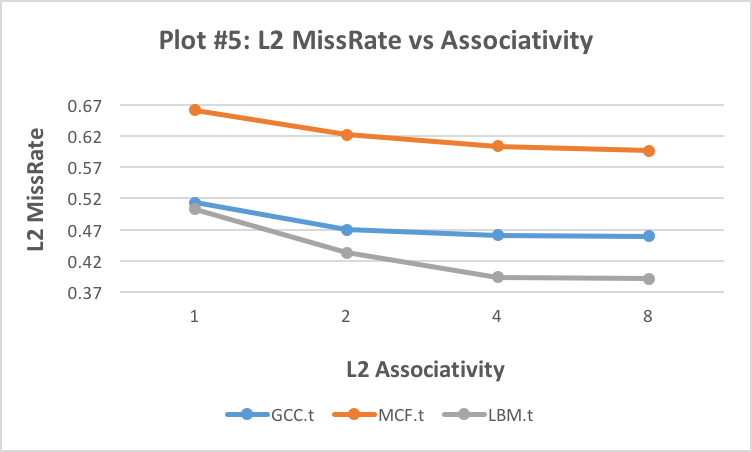
|  |  |  |  |
| --- | --- | --- | --- |
|  | **L2 Cache Miss Rates** | | |
| **L2 Cache Size** | **GCC.t** | **MCF.t** | **LBM.t** |
| **128 KiB** | 0.459704 | 0.59623 | 0.391004 |
| **256 KiB** | 0.456172 | 0.561573 | 0.359462 |
| **512 KiB** | 0.455574 | 0.533018 | 0.35941 |
| **1024 KiB** | 0.45546 | 0.509986 | 0.35941 |



**Plot #5:**

Fix block size at 64B, L1 cache size at 16KiB, L1 associativity at 4 and the replacement policy to be LRU. Assume that the L2 Cache is always non-inclusive. Fix the L2 cache size at 128KiB. Vary L2 associativity between 1, 2, 4 and 8. Plot the L2 cache miss rates. The plot should have 4 data points per benchmark.

|  |  |  |  |
| --- | --- | --- | --- |
|  | **L2 Cache Miss Rates** | | |
| **L2 Associativity** | **GCC.t** | **MCF.t** | **LBM.t** |
| **1** | 0.513062 | 0.661931 | 0.502475 |
| **2** | 0.469661 | 0.621907 | 0.432523 |
| **4** | 0.460858 | 0.603782 | 0.393176 |
| **8** | 0.459704 | 0.59623 | 0.391004 |



**Exploring the Inclusion Property Choices:**

**Plot #6:**

Fix the block size at 64B, the L1 associativity at 4 and the L2 associativity at 8. Vary L1 cache size between 8KiB, 16KiB, 32KiB and 64KiB. For each resulting configuration, vary the L2 cache size between 128KiB, 256KiB, 512KiB and 1MB. There are a total of 16 configurations. Plot the number of cache misses resulting in a memory read for each configuration for each inclusion policy (inclusive, exclusive and non-inclusive). Note that for each benchmark this plot will have 3 data series (one per inclusion policy) and each data series will have 16 points (one per configuration).

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **GCC.t** | | | **MCF.t** | | | **LBM.t** | | |
| **Cache Sizes** | **NON** | **INCL** | **EXCL** | **NON** | **INCL** | **EXCL** | **NON** | **INCL** | **EXCL** |
| **L1=8KiB, L2=128 KiB** | 65092 | 65247 | 65088 | 921339 | 921391 | 919790 | 313461 | 313673 | 310353 |
| **L1=8KiB, L2=256 KiB** | 65049 | 65066 | 65049 | 895405 | 895413 | 894919 | 302528 | 302528 | 302522 |
| **L1=8KiB, L2=512 KiB** | 65045 | 65045 | 65045 | 874010 | 874010 | 873810 | 302517 | 302517 | 302517 |
| **L1=8KiB, L2=1024 KiB** | 65045 | 65045 | 65045 | 856786 | 856786 | 856676 | 302517 | 302517 | 302517 |
| **L1=16KiB, L2=128 KiB** | 55257 | 55791 | 55245 | 909403 | 909504 | 906118 | 313924 | 314172 | 310308 |
| **L1=16KiB, L2=256 KiB** | 55214 | 55298 | 55213 | 883493 | 883539 | 882428 | 302532 | 302532 | 302518 |
| **L1=16KiB, L2=512 KiB** | 55210 | 55222 | 55210 | 862150 | 862152 | 861758 | 302513 | 302513 | 302513 |
| **L1=16KiB, L2=1024 KiB** | 55210 | 55210 | 55210 | 844924 | 844924 | 844712 | 302513 | 302513 | 302513 |
| **L1=32KiB, L2=128 KiB** | 53166 | 54086 | 53142 | 895795 | 896031 | 888605 | 313855 | 314143 | 309637 |
| **L1=32KiB, L2=256 KiB** | 53129 | 53251 | 53120 | 869800 | 869860 | 867386 | 302532 | 302532 | 302517 |
| **L1=32KiB, L2=512 KiB** | 53118 | 53134 | 53118 | 848489 | 848503 | 847620 | 302513 | 302513 | 302513 |
| **L1=32KiB, L2=1024 KiB** | 53118 | 53118 | 53118 | 831267 | 831267 | 830848 | 302513 | 302513 | 302513 |
| **L1=64KiB, L2=128 KiB** | 52217 | 53881 | 52187 | 867973 | 873907 | 853657 | 305996 | 306305 | 292953 |
| **L1=64KiB, L2=256 KiB** | 52175 | 52424 | 52173 | 840858 | 841613 | 835127 | 292616 | 292616 | 292599 |
| **L1=64KiB, L2=512 KiB** | 52171 | 52195 | 52171 | 819600 | 819703 | 817695 | 292599 | 292599 | 292599 |
| **L1=64KiB, L2=1024 KiB** | 52171 | 52171 | 52171 | 802381 | 802396 | 801492 | 292599 | 292599 | 292599 |

**Plot #7:**

Fix the block size at 64B, the L1 associativity at 4 and the L2 associativity at 8. Vary L1 cache size between 8KiB, 16KiB, 32KiB and 64KiB. For each resulting configuration, vary the L2 cache size between 128KiB, 256KiB, 512KiB and 1MB. There are a total of 16 configurations. Plot the number of cache misses resulting in a memory read for each configuration for each inclusion policy (inclusive, exclusive and non-inclusive). Note that for each benchmark this plot will have 3 data series (one per inclusion policy) and each data series will have 16 points (one per configuration).